ABSTRACT OF THE DISCLOSURE

A frame synchronization detecting circuit is provided which is capable of efficiently reducing power consumption in a hunting state.

The frame synchronization detecting circuit composed of a frame synchronization pattern detecting circuit, a receiver frame counter and a state transition judging circuit has an in-house phase frame counter adapted to produce a receiving frame enable signal having a pulse width of "$2\delta+\alpha$" (nsec) in a timing manner that an in-house frame pulse (FP) rises at a midpoint of the pulse width of the receiving frame enable signal. While the frame synchronization detecting circuit is in a hunting state in which a frame synchronization pattern is being sought by the frame synchronization pattern detecting circuit, only when the above receiving frame enable signal is in an enable state, a synchronization clock is fed to the frame synchronization pattern detecting circuit and the state transition judging circuit.